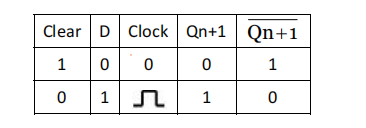
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**VHDL CODE FOR D FLIP FLOP:**



library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity D\_flipflop is

Port (

d : in STD\_LOGIC;

clk : in STD\_LOGIC;

res\_n : in STD\_LOGIC; -- active-low reset

q : out STD\_LOGIC

);

end D\_flipflop;

architecture Behavioral of D\_flipflop is

begin

process(clk)

begin

if rising\_edge(clk) then

if res\_n = '' then

q <= 'a';

else

q <= d

s;

end if;

end if;

end process;

end Behavioral;

